IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-23848.1
	Theodore W. Houston	Art Unit: 2825
Serial No:		Examiner: T. Do
Filed:	August 2, 2001	
For:	System and Method for Controlling Leakage Current in an Integrated Circuit Using Current Limiting Devices	

PRELIMINARY AMENDMENT

"EXPRESS MAILING" Mailing Label No. **EL645453679**. Date of Deposit: **August 2, 2001**. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown above and is addressed to. Ass't Commissioner for Patents, Washington, D.C. 20231.

Robin E. Barnum

Ass't Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to examination of this divisional application, please amend the above-identified patent application as follows:

IN THE TITLE:

Please change the title to: -- System and Method for Controlling Current in an Integrated Circuit--.

IN THE SPECIFICATION:

Rewrite the paragraph at page 4, lines 16 and 17 as follows:

--FIGURE 6 is a cross-sectional elevational diagram of a transistor constructed using the techniques of the present invention;--

Rewrite the paragraph at page 4, lines 18 and 19 as follows:

--FIGURE 7 is a schematic illustration of an integrated circuit constructed using systems and techniques of the present invention; and--

Add the following paragraph at page 4, following line 19:

--FIGURE 8 is a schematic illustration of an integrated circuit constructed using an additional embodiment of this invention.--

IN THE CLAIMS:

Please cancel Claims 1-18 without prejudice and add the following new Claims 19-40:

--19. An integrated electronic system comprising:

a first current carrying transistor;

means for adjusting a threshold voltage of the current carrying transistor in response to a control voltage; and

means for supplying the control voltage connected to the means for adjusting the threshold voltage, operable to supply a first control voltage to select a low power mode and a second control voltage to select a higher power mode relative to the first low power mode.

20. The integrated electronic system of claim 19 wherein the current carrying transistor comprises a back gate, and wherein the means for adjusting is a connection between the back gate and the means for supplying the control voltage.

21. The integrated electronic system of claim 20 wherein the back gate comprises a substrate associated with the current carrying transistor.

22. The integrated electronic system of claim 20 wherein the back gate comprises a tank region associated with the current carrying transistor.

23. The integrated electronic system of claim 20 wherein the back gate comprises a body region of the current carrying transistor.

24.The integrated electronic system of claim 20 wherein the back gate comprises a conductor separated by a dielectric from the channel region of the current carrying transistor.

25. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is a bond pad.

26. The integrated electronic system of claim 19, wherein the means for supplying the control voltage comprises selection circuitry on the same integrated circuit as is the current carrying transistor.

27. The integrated electronic system of claim 19, wherein the means for supplying the control voltage comprises selection circuitry connected to receive a clock signal, wherein the control voltage is selected based on clock period of the clock signal.

28. The integrated electronic system of claim 27, wherein the selection circuitry further comprise comparison circuitry connected to receive a signal passed through the current carrying transistor and to compare this signal the clock period.

29. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is operable to be selected in a permanent fashion.

30. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is operable to dynamically select a control voltage in response to a change in an operation condition of the integrated electronic system.

31. The integrated electronic system of claim 19, wherein a logic gate connected to provide an input to the current carrying transistor does not have a corresponding means for controlling a threshold voltage.

32. The integrated electronic system of claim 19, wherein the means for adjusting the threshold voltage of the current carrying transistor is a source resistance transistor connected between the current carrying transistor and a supply voltage, a control gate of the source resistance transistor being connected to the means for supplying a control voltage.

33. The integrated electronic system of claim 32, wherein the source resistance transistor is connected in parallel with a conductive element.

34. The integrated electronic system of claim 33, wherein the conductive element is a transistor.

35. The integrated electronic system of claim 32, wherein the source resistance transistor comprises a source region, a drain region, and a channel region, said source, drain, and channel region being of the same conductivity type.

36. An integrated electronic system comprising:

a first current carrying transistor;

means for adjusting a threshold voltage of the first current carrying transistor in response to a first control voltage;

a second current carrying transistor connected in series to the first current carrying transistor;

means for adjusting a threshold voltage of the second current carrying transistor in response to a second control voltage; and

means for independently supplying the first control voltage and the second control voltage.

37. An integrated electronic system comprising:

a plurality of transistors connected in series between a first voltage source terminal and a second voltage terminal;

a first transistor of the plurality of transistors being a first current carrying transistor having a control gate and a back-gate, with means for adjusting the threshold voltage of the first current carrying transistor by connecting the back-gate to a selected one of a first plurality of voltage terminals; and

a second transistor of the plurality of transistors being a source resistance transistor having a control gate, with means for connecting the control gate of the source resistance transistor to a selected one of a second plurality of voltage terminals.

38. The system of Claim 37, wherein the back-gate connection comprises a connection to the substrate associated with the first current carrying transistor.

39. The system of Claim 37, wherein a third transistor of the plurality of transistors is a second current carrying transistor having a control gate and a back-gate, with means for adjusting the threshold voltage of the second current carrying transistor by connecting the back-gate of the second current carrying transistor to a selected one of a third plurality of voltage terminals.

40. The integrated system of claim 39 wherein the first current carrying transistor is an n-channel transistor and the second current carrying transistor is a p-channel transistor.--

REMARKS

Prior to examination of this application, please amend the claims as indicated above. Claims 19-40 are pending in this application.

The application has been further amended at page 4 to provide a brief description of FIGURE 8. This brief description corresponds to the original application at page 16, lines 9 to 10.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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Amendments/Claims as They Stand Revised/New

SPECIFICATION:

FIGURE 6 is a cross-sectional elevational diagram of a transistor constructed using the techniques of the present invention;

FIGURE 7 is a schematic illustration of an integrated circuit constructed using systems and techniques of the present invention; and

FIGURE 8 is a schematic illustration of an integrated circuit constructed using an additional embodiment of this invention.

CLAIMS:

19. An integrated electronic system comprising:

a first current carrying transistor;

means for adjusting a threshold voltage of the current carrying transistor in response to a control voltage; and

means for supplying the control voltage connected to the means for adjusting the threshold voltage, operable to supply a first control voltage to select a low power mode and a second control voltage to select a higher power mode relative to the first low power mode.

20. The integrated electronic system of claim 19 wherein the current carrying transistor comprises a back gate, and wherein the means for adjusting is a connection between the back gate and the means for supplying the control voltage.

21. The integrated electronic system of claim 20 wherein the back gate comprises a substrate associated with the current carrying transistor.

22. The integrated electronic system of claim 20 wherein the back gate comprises a tank region associated with the current carrying transistor.

23. The integrated electronic system of claim 20 wherein the back gate comprises a body region of the current carrying transistor.

24.The integrated electronic system of claim 20 wherein the back gate comprises a conductor separated by a dielectric from the channel region of the current carrying transistor.

25. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is a bond pad.

26. The integrated electronic system of claim 19, wherein the means for supplying the control voltage comprises selection circuitry on the same integrated circuit as is the current carrying transistor.

27. The integrated electronic system of claim 19, wherein the means for supplying the control voltage comprises selection circuitry connected to receive a clock signal, wherein the control voltage is selected based on clock period of the clock signal.

28. The integrated electronic system of claim 27, wherein the selection circuitry further comprise comparison circuitry connected to receive a signal passed through the current carrying transistor and to compare this signal the clock period.

29. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is operable to be selected in a permanent fashion.

30. The integrated electronic system of claim 19, wherein the means for supplying the control voltage is operable to dynamically select a control voltage in response to a change in an operation condition of the integrated electronic system.

31. The integrated electronic system of claim 19, wherein a logic gate connected to provide an input to the current carrying transistor does not have a corresponding means for controlling a threshold voltage.

32. The integrated electronic system of claim 19, wherein the means for adjusting the threshold voltage of the current carrying transistor is a source resistance transistor connected between the current carrying transistor and a supply voltage, a control gate of the source resistance transistor being connected to the means for supplying a control voltage.

33. The integrated electronic system of claim 32, wherein the source resistance transistor is connected in parallel with a conductive element.

34. The integrated electronic system of claim 33, wherein the conductive element is a transistor.

35. The integrated electronic system of claim 32, wherein the source resistance transistor comprises a source region, a drain region, and a channel region, said source, drain, and channel region being of the same conductivity type.

36. An integrated electronic system comprising:

a first current carrying transistor;

means for adjusting a threshold voltage of the first current carrying transistor in response to a first control voltage;

a second current carrying transistor connected in series to the first current carrying transistor;

means for adjusting a threshold voltage of the second current carrying transistor in response to a second control voltage; and

means for independently supplying the first control voltage and the second control voltage.

37. An integrated electronic system comprising:

a plurality of transistors connected in series between a first voltage source terminal and a second voltage terminal;

a first transistor of the plurality of transistors being a first current carrying transistor having a control gate and a back-gate, with means for adjusting the threshold voltage of the first

current carrying transistor by connecting the back-gate to a selected one of a first plurality of voltage terminals; and

a second transistor of the plurality of transistors being a source resistance transistor having a control gate, with means for connecting the control gate of the source resistance transistor to a selected one of a second plurality of voltage terminals.

38. The system of Claim 37, wherein the back-gate connection comprises a connection to the substrate associated with the first current carrying transistor.

39. The system of Claim 37, wherein a third transistor of the plurality of transistors is a second current carrying transistor having a control gate and a back-gate, with means for adjusting the threshold voltage of the second current carrying transistor by connecting the back-gate of the second current carrying transistor to a selected one of a third plurality of voltage terminals.

40. The integrated system of claim 39 wherein the first current carrying transistor is an n-channel transistor and the second current carrying transistor is a p-channel transistor.